OIPE JC10 MAR 24 2003 ADEMARK OFFICE

Response #13 3-31-03 G. Artis

March 18, 2002

TO: Commissioner of Patents and Trademarks
Washington, D.C. 20231

FROM: George O. Saile, Reg. No. 19,572
28 Davis Ave.
Poughkeepsie, N.Y. 12603

SUBJECT:

Serial #:	09/587,465
File Date:	06/05/2000
Inventor:	LIN, JUNG-CHENG
Examiner:	SARKAR, ASOK K.
Art Unit:	2829
New Title:	METHOD OF FORMING MULTILAYER DIFFUSION BARRIER FOR COPPER INTERCONNECTIONS

OFFICE ACTION

This is a response to an Office Action, mail dated December 18, 2002, Paper No. 12. Please amend the above identified application for patent as follows.

RECEIVED TECH... 2800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on March, 18 2003.

Signature _____ Date: 3/18/03

Stephen B. Ackerman, Reg. No. 37,761

REMARKS

Examiner Asok K. Sarkar is thanked for carefully examining and reviewing the subject patent application. The claims and the specifications have been amended in accordance with the Examiner's kind suggestions, and all claims are now believed to be in condition for allowance.

SUMMARY OF THE APPLICANT'S CLAIMED INVENTION

It is a general object of the present invention to provide an improved method to form a copper diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing, for 0.10 micron nodes in MOSFET and CMOS applications. The diffusion barrier is formed by first depositing a tungsten nitride bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and then finally depositing a final top layer of tungsten. This invention is used to manufacture reliable metal interconnects and contact vias in the fabrication of MOSFET and CMOS devices for both logic and memory applications. The copper diffusion barrier formed, W/WSiN/WN, passed a stringent barrier thermal reliability test at 400 ^{0}C. For pure single barrier layers, i.e., single layer WN, these

exhibited copper punch through or copper spiking during the stringent barrier thermal reliability test at 400 °C.

CLAIM REJECTIONS - 35 USC 103:

Reconsideration of the rejection of claims 1 - 10, 12 - 23, 25 and 26 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Danek et al.(US 5,942,799, hereafter referred to as Danek), and Hsu et al.(US 6,194,310 B1, US 6,054,382, hereafter referred to as Hsu), is requested, based on the following.
(Ref. Office Action, dated 12/18/2002, Paper No.12, Sect.4)

The prior art references of Edelstein, Danek and Hsu neither teach nor suggest, the Applicant's claimed invention. Edelstein teaches methods of forming copper wiring, as its title indicates, "COPPER INTERCONNECTION STRUCTURE INCORPORATING A METAL SEED LAYER." The focus is on forming copper alloys and other metals as seed layers, and either teaches nor suggests the Applicant's claimed invention teaching a three component metal barrier layer. However, most dual damascene processes for forming interconnection wiring do teach the incorporation of a metal diffusion barrier, as taught by Edelstein.

Agree with Examiner that Edelstein fails to teach the method of the Applicant's claimed invention, namely: the formation of an improved copper metal diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing with 0.10 micron nodes for MOSFET and CMOS applications. Edelstein fails to teach the Applicant's method of: forming a diffusion barrier by depositing a tungsten nitride, WN, bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and depositing a final top layer of tungsten, W.

Politely disagree with the Examiner concerning the Examiner's statement, "it would have been obvious ...to modify Edelstein's barrier layer structure" by applying the teaching of both Danek and Hsu. Exactly what barrier material or materials yield good adhesion and barrier properties, and enhances both copper seed deposition and copper electro-plating? In addition, it is not obvious exactly what processing conditions are optimum to achieve new and unexpected results. The Applicant's claimed invention teaches all of the above, and answers the questions above directly, without broad assumptions.

Also, agree with the Examiner's statement (ref. Paper 7, 06/25/2002), that "Danek and Hsu fail to expressly teach the processing steps of providing insulator/dielectric layers, patterning and etching to form trench to be filled by Cu seed layers, patterning and etching to form trench to be filled by Cu seed layer and ECD Cu layer." Danek's disclosure teaches the ease of deposition by a chemical vapor deposition, in a multi-station module or cluster tool. In contrast, the Applicant's claimed invention teaches specifically the three component barrier layer: W/WSiN/WN, whereas Danek's invention teaches alternating layers of material (A) and material (B).

An effort was made to limit the scope of Applicant's Claim 1, namely, to the specific three component layering of the barrier layers, with specific processes and specific thickness ranges, to avoid inteference with the Prior Art cited by the Examiner. Agree with the Examiner's statement, "Regarding claims 4-7 and 17-20, Edelstein does not teach the deposition process or the thickness of the layers of the composite barrier layer." Also the Examiner's statement, "Regarding claims 8 and 21, Edelstein fails to teach the method of forming the WSiN layer."

The applicant's claimed invention is improvement over prior art, in that, the Applicant's claimed invention teaches a method that saves some processing steps. The Applicant's claimed invention teaches a deposition of WN, bottom layer, then silane soak for WSiN (no need for another deposition layer) , then followed by deposition of W, top layer. Only two deposition steps are required, instead of three.

Agree with the Examiner that Danek and Hsu fail to teach the Applicant's dual damascene process integration with a barrier layer.

Politely disagree with the Examiner, in that the Applicant's invention demonstrates diligence and reduction to practice in the processing conditions found in the depend claims. Also, there may exist similar process steps related to general semiconductor processing and dual damascene processing. There are many common elements amongst the Prior Art that the Examiner has cited.

Reconsideration of the rejection of claims 11 and 24 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as

Edelstein), in view of Danek et al.(US 5,942,799, hereafter referred to as Danek), and Hsu et al.(US 6,194,310 B1, US 6,054,382, hereafter referred to as Hsu), as applied to claims 1 and 14 above, and further in view of Yu et al.(US 6,291,332 B1) and Hsu et al.(US 6,054,382), is requested based on the following.
(Ref. Office Action, dated 12/18/2002, Paper No.12, Sect.5)

Agree with the Examiner's statement, "Edelstein in view of Danek and Hsu fails to teach ECD copper deposited on seed layer and barrier layer with fine gained <111> structure." This is a key point that these prior art disclosures neither teach nor suggest the Applicant's claimed invention. In addition, Edelstein fails to teach the method of forming a WSiN layer.

Furthermore, Yu, as the title of the disclosure states, "Electroless Plated Semiconductor Vias and Channels," teaches a plating method for dual damascene, emphasizes the need for the copper seed layer to have <111> crystal orientation, as the Applicant's claimed invention teaches and achieves. Yu's disclosure teaches only some common barrier layer materials, with elemental W being the

only material common to just one layer of the Applicant's claimed invention.

Agree with the Examiner that fine grain <111> for seed and plated copper is desirable, but by what methods, can one achieve a <111> copper seed layer consistently and reliably on a dual damascene barrier layer. The Applicant's claimed invention demonstrates the development of a process that achieves good properties in the seed and plated copper, and that has passed stringent reliability tests for copper interconnect wiring. Politely disagree with the Examiner regarding the modification of "Edelstein's ECD Cu deposition", as being obvious.

In summary, the Applicant's claimed invention teaches a deposition of WN, bottom layer, then a silane soak, and then followed by deposition of W, top layer. Only two deposition steps are required, instead of three. The sequence, selection of material and processing of the Applicant's claimed invention are critical for good adhesion properties, good <111> copper plating and good electrical properties of the inlaid plated copper interconnects.

In conclusion, for state-of-the-art advanced applications in silicon technology, the Applicant's claimed invention is believed to be patentable over Edelstein, Danek, Hsu, Yu and Hsu, because there seems to be insufficient basis for concluding that the modification of Prior Art disclosures would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination.

FINAL REMARKS

The Examiner Asok K. Sarkar is again thanked for carefully examining and reviewing the subject patent application. The specifications and claims have been reviewed in accordance with all the Examiner's kind suggestions, and after amending the specifications and claims in accordance with the Examiner's helpful suggestions, all claims are now believed to be in condition for allowance.

All rejected Claims 1 - 26 are now believed to be in allowable condition, and allowance **is so** requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned, "Version With Markings to Show Changes Made."

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

Stephen B. Ackerman,

Reg. No. 37,761